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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,880	03/30/2004	Koji Hirose	57810-097	2498
<div>7590 11/27/2007 McDERMOTT, WILL & EMERY 600 13th Street, N.W. Washington, DC 20005-3096</div>			<div>EXAMINER SITTA, GRANT</div>	
			<div>ART UNIT 2629</div>	<div>PAPER NUMBER</div>
			<div>MAIL DATE 11/27/2007</div>	<div>DELIVERY MODE PAPER</div>

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/811,880	Applicant(s) HIROSAWA, KOJI	
	Examiner Grant D. Sitta	Art Unit 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 September 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 and 13-21 is/are rejected.
- 7) ☐ Claim(s) 11, 12, 22 and 23 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>3/30/2004</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-7, 10, 13-18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moon et al (US 7,106, 292), hereinafter Moon.

4. In regards to claim 1, Moon discloses the limitations of a plurality of stages (fig. 16) of shift register circuits (fig. 16, SRC1, SCR2, SCR3, SCR4) for sequentially driving a plurality of drain lines for supplying a video signal to pixels (Fig. 16, Vdis); Examiner notes while Moon discloses drivers used for rows it would be obvious to one skilled in

the art to substitute row and column drivers. Also, Applicant references to using gate lines and drain lines in the Applicant's admitted prior art "a conventional shift register circuit having an inverter circuit of resistance load type is known. The shift register circuit is used with a circuit for driving the gate line and the drain line of, for example, a liquid crystal display."

Moon further teaches a first circuit section having a first transistor (Fig. 18 M2) of first conductivity type connected to a first potential (Fig. 18 VOFF) a second transistor (Fig. 18 M1) of first conductivity type connected to a second potential (Fig. 18 VON through M3), and a third transistor (Fig. 18 M6) of first conductivity type connected between a gate of said first transistor (Fig. 18 M2) and said second potential (Fig. 18 VON) for turning off said first transistor when said second transistor is in on state (Fig. 7, M1 and M2 are referred as pull-up part and pull-down part therefore one is in an on state while the other is in an off state. Also see, Col. 15 lines 1-20).

Lastly, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Moon to include the use of a plurality of first dummy shift registers arranged on the operation starting side of a plurality of stages of shift register circuits and not connected to a drain line. Examiner notes that the display area of most LCD displays extend past the edges of the display seen by the user. These edges of the display are concealed by borders, or frames, of the LC display apparatus. It would have been obvious to one skilled in the art to not have these connected to drain lines.

5. In regards to claim 2, Moon teaches a second dummy shift register circuit arranged on the side opposite to the operation starting side of said plurality of stages of shift register circuits and not connected to said drain line (fig. 16 Dummy stage 0 and dummy stage 1, col. 18, lines 37-6, Moon).

6. In regards to claim 3, Moon teaches wherein a start signal is input to the first stage of said plurality of stages of first dummy shift register circuits (Fig. 16, Dummy Stage 0).

7. In regards to claims 4 and 15, Moon teaches a first transistor (Fig. 18 M2), said second transistor (Fig. 18 M1) and said third transistor (Fig. M6) are a p-type field effect transistor (col. 13 lines, 50-70 "NMOS" or n-channel metal-oxide-semiconductor field effect transistor). Examiner notes it would have been an obvious matter of design choice to modify Moon's use of the NMOS by having replaced the NMOS with PMOS, or p-type field effect transistors, since applicant has not disclosed that having the PMOS solves any stated problem or is for any particular purpose and it appears that the shift registers would perform equally well with the NMOS.

8. In regards to claims 5 and 16, Moon teaches wherein a first capacitor is connected between the gate and a source of said first transistor. Examiner notes it is obvious to one skilled in the art to place capacitors between the gate and a source for

multiple reasons, such as to store a charge and also transistor have an inherent parasitic capacitance (col. 13, lines 60-70).

9. In regards to claims 6 and 17, Moon teaches wherein said third transistor (Fig. 18 M6) has two gate electrodes electrically connected to each other (Fig. 18 M4 gate and M2 gate).

10. In regards to claims 7 and 18, Moon teaches wherein said first transistor (Fig. 18 M2) is turned on in response to a clock signal (Fig. 18 STV col. 15, lines 1-20).

11. In regards to claim 13, Moon teaches a plurality of stages of shift register circuits (fig. 16 "Dummy Stage", "SRC1", "SRC2", "SRC3", "SRC4") for sequentially driving a plurality of drain lines for supplying a video signal to pixels (fig. 4 col. 11-12, lines 40-10); and a dummy shift register circuits (Fig. 16, "Dummy Stage") arranged on at least the side opposite to the operation starting side (Fig. 16. "Dummy Stage 1") of said plurality of stages of shift register circuits and not connected to said drain line (Fig. 16); wherein said shift registers and said dummy shift registers (Fig. 16 Dummy Stage", "SRC1", "SRC2", "SRC3", "SRC4") first circuit section having a first transistor ((fig. 18 M2)) of first conductivity type connected to a first potential (Fig. 18 VOFF), a second transistor (Fig. 18 M1) of first conductivity type connected to a second potential (Fig. 18 VON), and a third transistor (Fig. 18 M6) of first conductivity type connected between a gate of said first transistor (Fig. 18 M2) and said second potential (Fig. 18 VON) for turning off

said first transistor (Fig. 18 M1) when said second transistor is in on state (Fig. 7, M1 and M2 are referred as pull-up part and pull-down part therefore one is in an on state while the other is in an off state. Also see, Col. 15 lines 1-20).

12. In regards to claim 14, Moon teaches two stages of dummy shift register circuits not connected to said drain line and arranged on the operation starting side of said plurality of stages of shift register circuits (Fig. 16 "Dummy Stage 0" and "Dummy Stage 1").

13. In regards to claims 10 and 21, Moon teaches wherein said first circuit section further includes a fifth transistor (Fig. 18 M7) of first conductivity type connected between the gate of said first transistor (Fig. 18 M2) and a clock signal line (Gout[1]) for supplying a clock signal and operated to turn on in response to a signal turned on when said third transistor (Fig. 3 M6) is in off state ((col. 4-5 lines 50-20).

14. Claims 8, 9, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moon as applied to claims 1 and 13 above, and further in view of Hebiguchi et. al (US 6,295,046) hereinafter Hebiguchi.

In regards to claims 8 and 19. Moon discloses the limitations of claims 1 and 13

Moon differs from the claimed invention in that Moon does not disclose a diode-connected transistor between the gate of the first transistor and a clock signal.

However, Hebiguchi teaches a system and method for including a diode-connected transistor between the gate of the first transistor and a clock signal (Fig. 7 col. 5, lines 45-55 of Hebiguchi).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Moon to include the use of a diode-connected transistor as taught by Hebiguchi in order to resist noise interference as stated in (Fig. 7 col. 5, lines 45-55 of Hebiguchi).

15. In regards to claims 9 and 20, Hebiguchi discloses wherein said diode-connected fourth transistor has two gate electrodes electrically connected to each other (Fig. 7 "2" and the gate of the diode-connected transistor).

Allowable Subject Matter

16. Claims 11-12 and 22-23 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

17. The cited references have failed to teach Applicant's claimed inventions of claim 11 and 22:

"first circuit section includes a fourth transistor of first conductivity type connected to the gate of said first transistor and operated to turn on in response to a first signal, and a fifth transistor

of first conductivity type connected between said fourth transistor and said first potential and operated to turn on in response to a second signal turned off when said first signal is in on state."

18. The cited references also fail to teach Applicant's claim invention of claims 12 and 23: "wherein a second capacitor is connected between the source of said first transistor and a junction point between said fourth transistor and said fifth transistor."

Response to Arguments

19. Applicant's arguments filed 9/19/2007 have been fully considered but they are not persuasive.

20. In regards to Applicant's first contention that Moon does not teach the plurality of stages. Moon does teaches a first dummy stage and the mere duplication of parts for multiplied effect is generally considered obvious to one of ordinary skill in the art. (St. Regis Paper Co. v. Bemis Co., Inc., 193 USPQ 8, 11 (7th Cir. 1977)).

As recited on page 7, line 25, through page 8, line 8 of the pending application and page 10 of Applicant's Response to Arguments, "in the case where a display is fabricated by connecting the shift register circuits described above in a plurality of stages and connecting the plurality of stages of shift register circuits to the pixels constituting a display section, display irregularities may occur in an area corresponding

to the drain line connected to the second-stage one, from the operation start side, of the plurality of stages of shift register circuits of the display section."

Therefore, the mere duplicating of the dummy shift registers, as taught by Moon, for the purpose of preventing "display irregularities" would generally be considered obvious to one of ordinary skill in the art.

21. In regards to Applicant's second contention that a transistor for turning off the first transistor (corresponding to M2) of the present invention is not M6 (indicates as a third transistor of the present application), but M7. Examiner respectfully disagrees. As state in col. 15, lines 8-11 "Meanwhile, the voltage of the third node N3 rises to the second power voltage Von by the transistor M6 before the scan start signal STV is inputted into the pull-down driver part 174, and the transistor M2 is turned on." Since M6 is connected to the gate of M2 and turns M2 on. It stands to reason that M6 would also turn off M2.

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure: Washino (6,724,361) is cited for teaching a shift register display device with the driving pulse synchronized with a clock pulse. Lee (5,648,790) is cited for teaching shift register stages with two dummy stages. Pathak (7,167,404) is cited for teaching two dummy stages in a programmable logic device.

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Grant D. Sitta whose telephone number is 571-270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Grant D. Sitta

November 20, 2007


AMARE MENGISTU
SUPERVISORY PATENT EXAMINER